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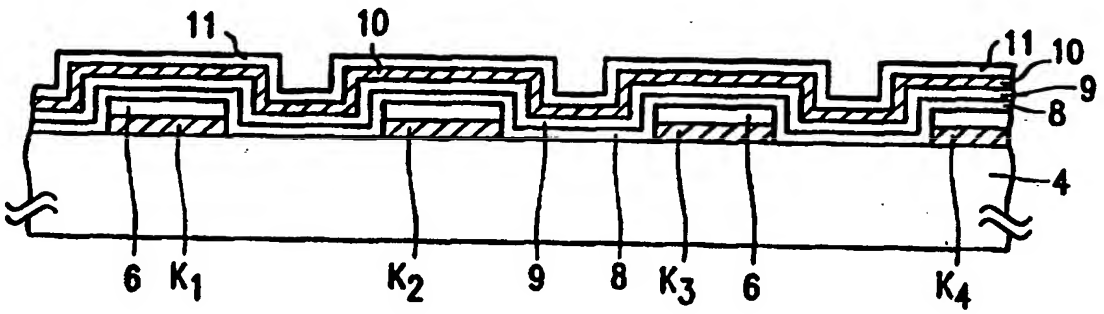

(57) Abstract

The invention relates to an erasable non-volatile memory in which a diode is formed at each point of intersection between the x-selection lines (K_i) and y-selection lines (R_j), of which diode the anode and cathode are conductively connected to the x- and y- selection lines. The diodes are formed in hydrogenated amorphous silicon or silicon compounds such as amorphous $Si_{1-x}Ge_x$. Writing takes place by means of a current pulse through selected diodes. The current in the forward direction becomes much lower, for example a few hundred times lower, than in diodes which are not selected, probably owing to degradation in the semiconductor material. The diodes may be returned to their original state again (i.e. be erased) through heating, for example at a temperature of 200 °C during 100 minutes. Preferably, the diodes are formed by Schottky diodes because the characteristic in the reverse direction does not (substantially) change in this type of diode. The Schottky diodes may be formed in the transitional region between the amorphous intrinsic semiconductor material (6) and the selection lines (K_i).

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Programmable, non-volatile memory device, and method of manufacturing such a device.

The invention relates to a programmable, non-volatile memory device (PROM), comprising a system of programmable non-volatile memory cells arranged in a matrix of rows and columns and provided with a first set of selection lines parallel to the columns and with a second set of selection lines parallel to the rows, a memory cell being associated with each point of intersection between the selection lines. The invention also relates to a method of manufacturing such a device.

Programmable semiconductor memories or PROMs are known in various shapes. One of the earliest PROM types made use of fuses, where programming of a selected cell implies that the connection between a word line and a bit lines is broken in that the fuse is melted. These memories may be readily manufactured by generally known i.c. techniques, but they have the disadvantage that information once written cannot be erased any more. This means that a new chip is to be used for writing new data. In addition, the cells themselves cannot be tested during production and it is necessary to provide extra test cells on the chip which cannot be utilized for the memory. Another type of programmable memories is known under names such as EEPROM, EPROM, Flash EPROM. Each memory cell here comprises an MOS transistor with floating gate. The information is written in the form of electric charge at the floating gate and thus determines the threshold voltage of the transistor. These memories are erasable in principle, which means that separate test cells are unnecessary. A disadvantage is that the memory cells are comparatively large, which renders it difficult to manufacture memories with a very large number of bits. A third type of programmable memories, also erasable, is based on a resistance change in materials upon the transition between the crystalline and the non-crystalline state. Such memories are known inter alia under the abbreviated designation MIM (Metal-Insulator-Metal). These memories require for each cell besides the MIM element also a selection element such as a transistor or a diode. In addition, a chalcogenide material which does not form part of standard silicon processes is often used for the switchable element.

The invention has for its object inter alia to provide a programmable semiconductor memory which is erasable and which has a very high density. The invention further has for its object to provide such a memory which can be manufactured by silicon techniques which are known per se.

A programmable non-volatile memory device of the kind described in the opening paragraph, according to the invention, is characterized in that each memory cell is exclusively formed by a diode whose anode and cathode are each conductively connected to a selection line, at least one of the anode and cathode regions comprising a layer of hydrogenated, silicon-containing amorphous semiconductor material. Experiments have shown that it is possible, for example in a rectifying junction in hydrogenated amorphous silicon, for the current to be changed in the forward direction in that a large current is passed across the junction during a short time. The current in the forward direction is found to be very strongly reduced then compared with a non-stressed diode. It is not clear at this moment what the physical background of this effect is. Probably degradation occurs in the material owing to the generation of additional states within the forbidden band. These states can be eliminated again through heating. Each diode in a matrix of diodes may or may not be programmed by means of current, depending on the information to be written, corresponding to a "1" or a "0". In contrast to a fuse memory, no separate selection element is necessary now for each cell. In addition, each diode can be returned to its original state again through a heating step in which the degradation in the semiconductor material is eliminated. This renders it possible to test each cell itself after production, and separate test cells are unnecessary.

An important embodiment of a device according to the invention with which a memory of maximum density can be obtained is characterized in that the layer of semiconductor material forms a stack with the selection lines at the area of the intersection between the selection lines and is connected at the upper side to one of the selection lines and at the lower side to the other selection line which crosses the former selection line.

In a simple embodiment, the diode is formed by a p-i-n diode, the letter i denoting "intrinsic" here, which means in practice a semiconductor material which is not purposely n-type or p-type doped. Materials may be used for the conductor tracks here which form an ohmic connection with the n-type and p-type zones of the p-i-n diodes.

A further embodiment of a device according to the invention is characterized in that at least one of the selection lines is formed by a metal track, and in that the diode is a Schottky diode arranged between this metal track and the layer of

semiconductor material. It was found in practice that a Schottky diode has the advantage that mainly the forward characteristic of the diode changes, whereas the current in the reverse direction does not change, or only slightly, which has advantages in reading. It is possible to use for the metal track, for example, a metal from the group: Mo, W, TiW, Pt, and Cr, which form good rectifying junctions with intrinsic αSi:H.

Various hydrogenated Si compounds may be taken for the amorphous semiconductor material, such as SiGe, SiC, or SiN. A simple embodiment is characterized in that the layer of semiconductor material is formed by a layer of hydrogenated amorphous silicon.

The properties of the amorphous semiconductor material, and thus of the diode to be formed, depend strongly on the circumstances under which the material is formed, in particular on the degree to which the dangling bonds are bound to hydrogen. According to the invention, a method of manufacturing a device of the kind described above is characterized in that the layer of amorphous semiconductor material is formed by means of PECVD (Plasma Enhanced CVD) at a temperature of at most 400 °C, and preferably at a temperature of at most approximately 250 °C. It was found that a suitable semiconductor material with a high concentration of hydrogen atoms bound to dangling bonds can be manufactured in this manner.

These and other aspects of the invention will be explained in more detail below with reference to a few embodiments. In the drawing:

Fig. 1 is a circuit diagram of an erasable PROM according to the invention;

Fig. 2 is a plan view of a portion of this memory;

Fig. 3 shows two steps in the manufacture of the memory shown in Figs. 1 and 2;

Fig. 4 shows I-V characteristics of a memory cell in the programmed and non-programmed state;

Fig. 5 shows the current in a programmed and a non-programmed diode as a function of the voltage; and

Fig. 6 is a cross-section of an alternative embodiment of a device according to the invention.

Fig. 1 represents the circuit diagram of a programmable semiconductor memory 1 according to the invention, comprising a matrix of programmable non-volatile memory cells M_{ij}, where i represents the row and j the column in the matrix. The device comprises a first set of selection lines K_1, K_2, K_3, etc., which are connected to a column decoder 2, and a second set of selection lines R_1, R_2, R_3, which are connected to a row decoder 3. The lines K_i and R_i form a system of crossing rods in which a memory element is associated with each point of intersection and can be addressed via selected lines.

According to the invention, each memory cell M_{ij} is exclusively formed by a diode whose anode is connected to a row selection line R_i and whose cathode is connected to a column selection line K_j, while at least one of the anode and cathode regions comprises hydrogenated, silicon-containing amorphous semiconductor material. In the present example, the diodes are formed by metal-semiconductor junctions or Schottky diodes between one of the selection lines and the layer of amorphous semiconductor material. Fig. 2 is a plan view of a portion of the memory. The vertical selection lines K_j are provided in a lower metal layer. The selection lines R_j are formed in a higher, wiring layer. The amorphous silicon forming the programmable diode in each point of intersection is provided between the selection lines and forms a vertical stack together with these lines in this embodiment.

Figs. 3a, 3b and 3c show the device in a cross-section taken on the line III-III in Fig. 2 in three stages of its manufacture. This starts (Fig. 3a) with a substrate 4, made of glass in this example, but which may also be made from an alternative electrically insulating material. The substrate may also be formed by a silicon oxide layer which covers a subjacent monocrystalline silicon body, in which the peripheral electronics, for example the decoders 2 and 3, may be provided, if so desired. A layer 5 of a suitable metal, for example Mo, with a thickness of approximately 100 nm is first formed on the surface of the substrate 4, followed by a deposition of a 100 nm thick layer 6 of amorphous silicon doped with hydrogen. Preferably, the layer 6 is deposited by means of PECVD (Plasma Enhanced CVD) at a low temperature (maximum 400 °C, preferably between 200 °C and 250 °C), for example from a mixture of SiH_4 and H_2. Owing to the low temperature, a comparatively high concentration of hydrogen can be obtained as is necessary for passivating the dangling bonds. Otherwise the Si material of the layer 6 is intrinsic, i.e. the concentration of n-type or p-type impurities has a low level which occurs naturally and is not purposely raised by means of a doping step. As a result, the Mo forms a rectifying junction with the Si.

The layer 6 is not essential and may be omitted when conventional lithography is used.

The αSi layer 6 is locally oxidized, for example in the manner as described in the article "Resistless high resolution optical lithography on silicon" by N. Kramer et al., published in Appl. Phys. Lett. 67 (20), 13 November 1995, pp. 2989/2991. In this method, the layer 6 is locally irradiated with UV (λ = 355 nm) in the air through openings in a shadow mask 7 defining the selection lines K_i. The αSi:H is oxidized through at least part of its thickness at the areas of the openings, whereby an oxide layer is formed which masks the subjacent portion of the Si against etching. The non-irradiated portion of the layer 6 is subsequently removed by etching; then the portions of the Mo layer 5 not covered by Si and the oxide layer on the remaining αSi of the layer 6 are also removed, so that the situation depicted in Fig. 3b is obtained, with the selection lines K_i being covered by lanes 6 of αSi:H. In a next step, a layer 8 of intrinsic amorphous silicon is first provided to a thickness of, for example, 400 nm, followed by a deposition of a layer 9 of n-type doped amorphous silicon with a thickness of, for example, 75 nm. The layers 8 and 9 are also doped with hydrogen and may be provided in the same manner as the layer 6. The n-type doping in the layer 9 may be provided during the deposition in that phosphine is added to the plasma. Then a second metal layer 10, in this example another Mo layer with a thickness of 75 nm, is provided, so as to form an ohmic junction with the - doped - Si of the layer 9. Finally a fourth layer 11 of αSi:H of approximately 75 nm is deposited. The selection lines R_i are defined in a manner analogous to that of the lines K in that the αSi layer 10 is locally oxidized at the areas of the lines R by means of UV radiation, whereupon the non-irradiated αSi of the layer 10 is removed by etching. The Mo layer is now brought into a pattern with the pattern thus obtained in the layer 10 acting as a mask, whereby the selection lines R_i are formed. Subsequently, the amorphous silicon of the layers 8 and 9 not covered by the remaining Mo of the layer 10 is removed, simultaneously with which the layer 11 can be removed. This in fact completes the memory matrix. The diodes are situated at the points of intersection between the lines K and the lines R, whereby a very compact configuration can be obtained.

Fig. 4 plots the current I in amps on the vertical axis as a function of the voltage V applied across a diode. Curve A represents the current of a non-programmed diode, with the voltage applied in the forward direction. This state may be regarded as a logic "0". When a very strong current is passed through the diode, degradation will occur in the intrinsic Si, as a result of which the current I becomes much lower in the case of a forward bias, i.e. curve B in Fig. 4. A specific value for this current is, for example, 1A/cm^2. The current value may be chosen within certain limits, for example in view of the

programming speed. Thus a stronger current may be chosen when the writing speed must be high. Given a voltage of 1 V, the difference in the forward current may be a factor 400, which may be used as a logic "1". The degradation is probably caused by the generation of defects in the intrinsic Si layer, which defects can be eliminated again through heating. It was found that heating to, for example, 200 °C for 100 minutes causes the diode to exhibit substantially the I-V characteristic A again. This effect can be utilized for erasing the memory. Curve C in Fig. 4 shows the I-V characteristic of a diode in the reverse bias state. This characteristic does not change substantially in the case of programming and/or erasing. Fig. 5 shows the ratio between the current through the diode in the programmed state and the current in the non-programmed state. As is evident from the drawing, this ratio depends strongly on the voltage and is of the order of 100 for a voltage of 1 V. The ratio is practically equal to 1 in the reverse bias state.

The memory may be tested after its manufacture in that each ceil is programmed and subsequently the memory is erased in the manner described above. Separate test cells are accordingly not necessary. In addition, it has important advantages for the reliability that the memory cells themselves can be tested. The diodes can be monitored during writing, the procedure being stopped when the current through the diode has been sufficiently reduced.

Fig. 6 is a cross-section of an embodiment of a non-volatile erasable programmable memory according to the invention in which the diodes are formed by p-i-n junctions in αSi:H. Corresponding components have been given the same reference numerals in Fig. 6 as in Fig. 3c for simplicity's sake. The memory matrix is provided on a substrate 3 again and comprises the column lines K_1, K_2, K_3, etc., which extend transversely to the plane of drawing over the substrate. These lines, for example made of Mo again, are covered with strip-shaped lanes of hydrogen-doped αSi which has been n-type or p-type doped with a suitable impurity. In this example, the lanes 16 are of the n-type and are doped with As or P atoms in a sufficiently high concentration such that the Mo lines K form conductive junctions with the amorphous Si lanes 16. The Mo lanes and the amorphous Si lanes 16 may be patterned in the same manner as the Mo lanes K and the amorphous Si lanes 6 in the preceding embodiment. The selection lines R_1 are formed by Mo lanes 10, of which one is shown in the drawing. A lane 17 of p-type doped αSi:H is present below the Mo lane 10, forming an ohmic junction with the Mo of the lane 10. The amorphous p-type lane 17 is separated from the amorphous n-type lanes 16 by an interposed strip 8 of amorphous intrinsic (not purposely n-type or p-type doped) Si. The layers, 10, 17 and 8 may be formed in the

same manner as the layers 10, 9 and 8 in the preceding embodiment. In the matrix shown in Fig. 6, a p-i-n diode is formed at each point of intersection between the lines K_i and the lines R_j (Mo lanes 10).

Writing and erasing of the memory of Fig. 6 may be effected in the manner as described with reference to the preceding embodiment.

It will be obvious that the invention is not limited to the embodiments described here but that many more variations are possible to those skilled in the art within the scope of the invention. Thus, instead of amorphous silicon, amorphous SiGe may be used, i.e. wherein part of the Si atoms are replaced by Ge atoms. Furthermore, suitable metals other than Mo may be used for the selection lines. A monocrystalline Si substrate may be used as the substrate 3, possibly provided with an integrated circuit comprising, for example, the necessary peripheral electronics for operating the memory. Furthermore, memories as described above may be stacked on top of one another in a multilayer structure, planarization layers being provided between the individual layers.

Claims:

1. A programmable, non-volatile memory device (PROM), comprising a system of programmable non-volatile memory cells arranged in a matrix of rows and columns and provided with a first set of selection lines parallel to the columns and with a second set of selection lines parallel to the rows, a memory cell being associated with each point of intersection between the selection lines, characterized in that each memory cell is exclusively formed by a diode whose anode and cathode are each conductively connected to a selection line, at least one of the anode and cathode regions comprising a layer of hydrogenated, silicon-containing amorphous semiconductor material.

2. A device as claimed in Claim 1, characterized in that the layer of semiconductor material forms a stack with the selection lines at the area of the intersection between the selection lines and is connected at the upper side to one of the selection lines and at the lower side to the other selection line which crosses the former selection line.

3. A device as claimed in Claim 1 or 2, characterized in that at least one of the selection lines is formed by a metal track, and in that the diode is a Schottky diode arranged between this metal track and the layer of semiconductor material.

4. A device as claimed in Claim 3, characterized in that the metal track is made from a metal from the group: Mo, W, TiW, Cr and Pt.

5. A device as claimed in Claim 1 or 2, characterized in that the diode is a p-i-n diode which is formed in the layer of semiconductor material.

6. A device as claimed in any one of the preceding Claims, characterized in that the layer of semiconductor material is formed by a layer of hydrogenated amorphous silicon.

7. A method of manufacturing a device as claimed in Claim 6, characterized in that the layer of amorphous semiconductor material is formed by means of PECVD at a temperature of at most 400 °C.

8. A method as claimed in Claim 7, characterized in that the deposition temperature is at most approximately 250 °C.

9. A method of operating a device as claimed in any one of the Claims 1 to 6, characterized in that the device is brought from a programmed state into the original state by means of a treatment at high temperature.

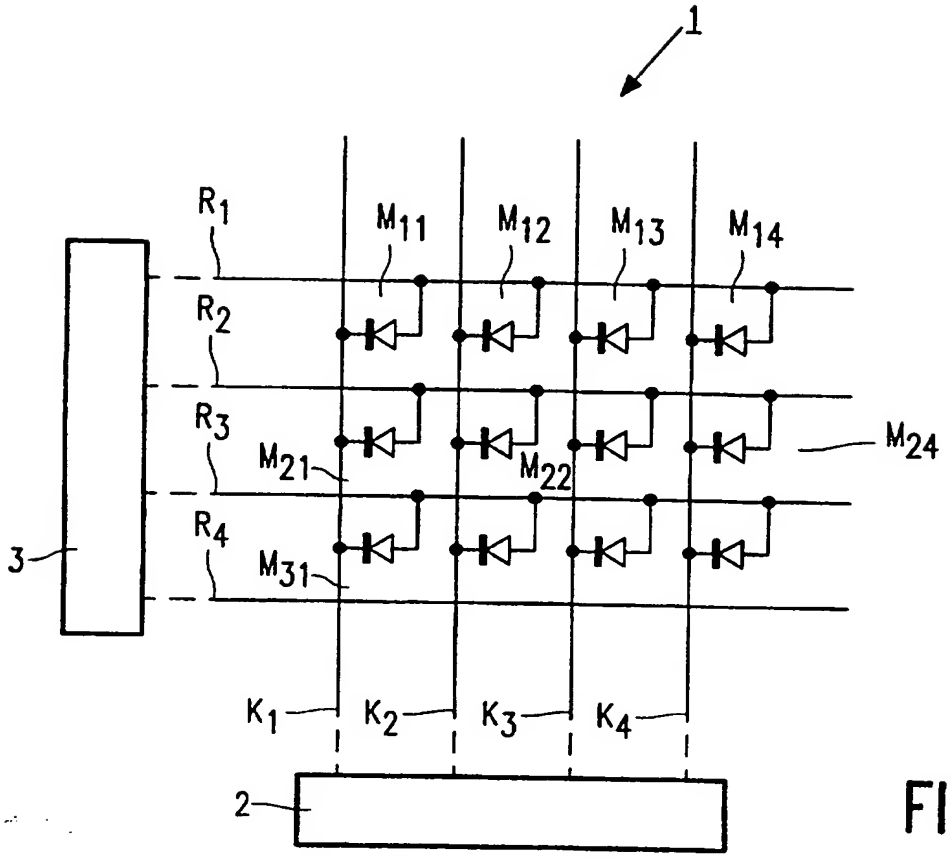

FIG. 1

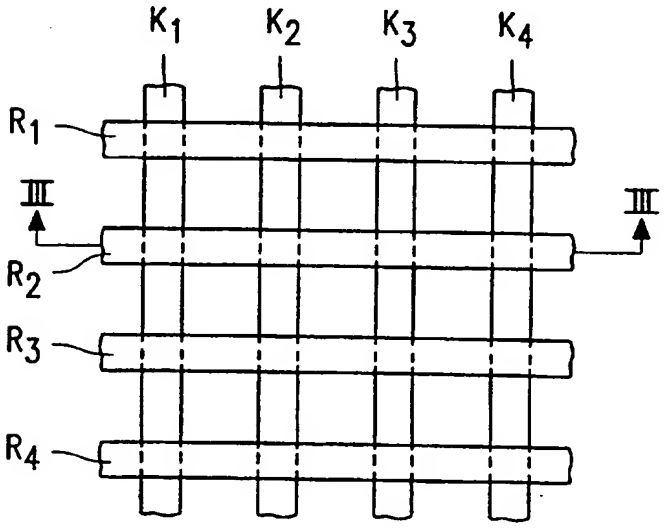

FIG. 2

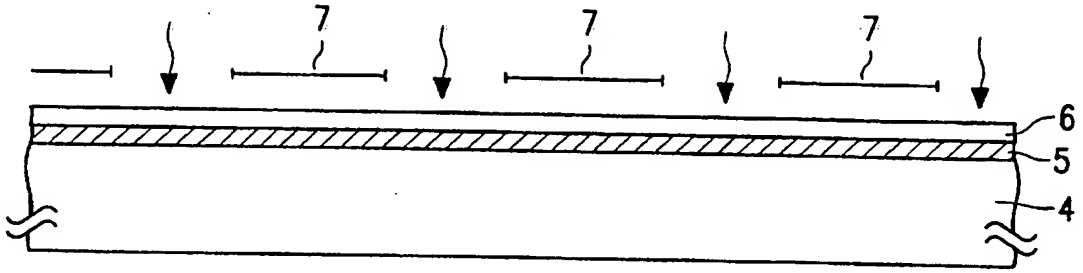

FIG. 3a

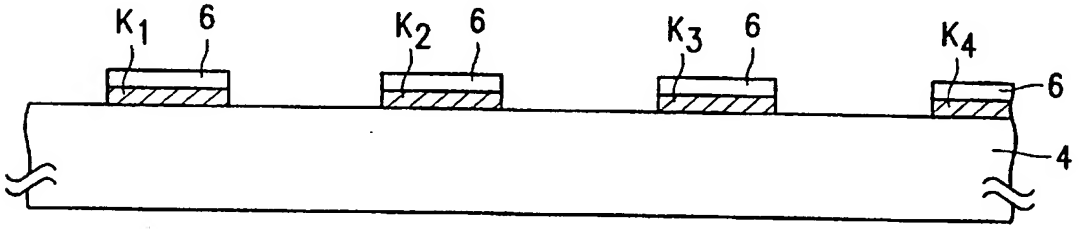

FIG. 3b

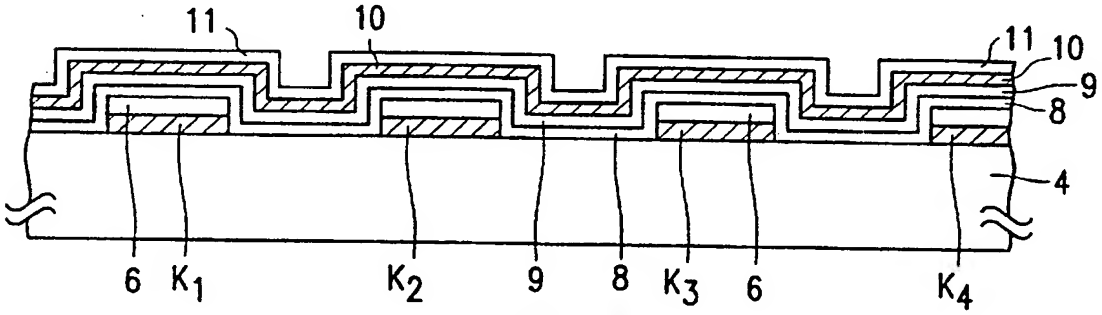

FIG. 3c

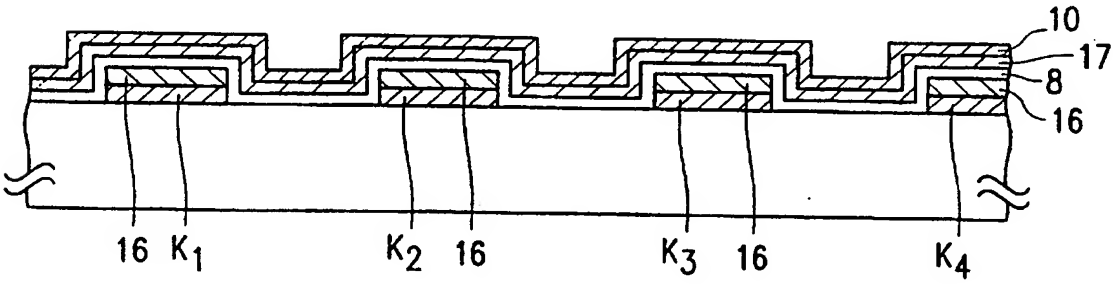

FIG. 6

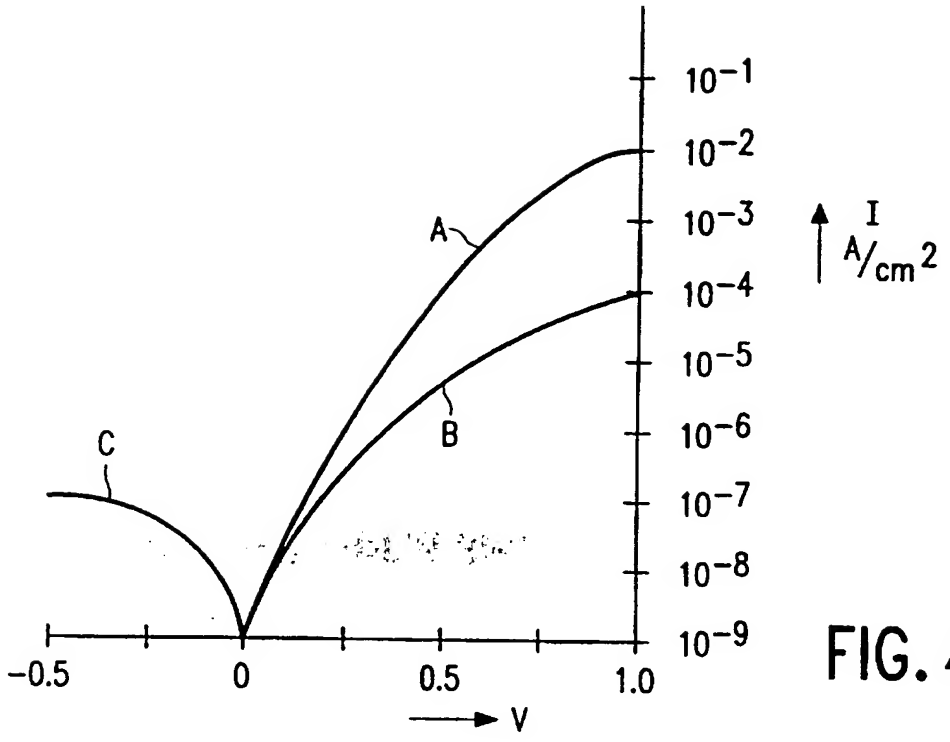

FIG. 4

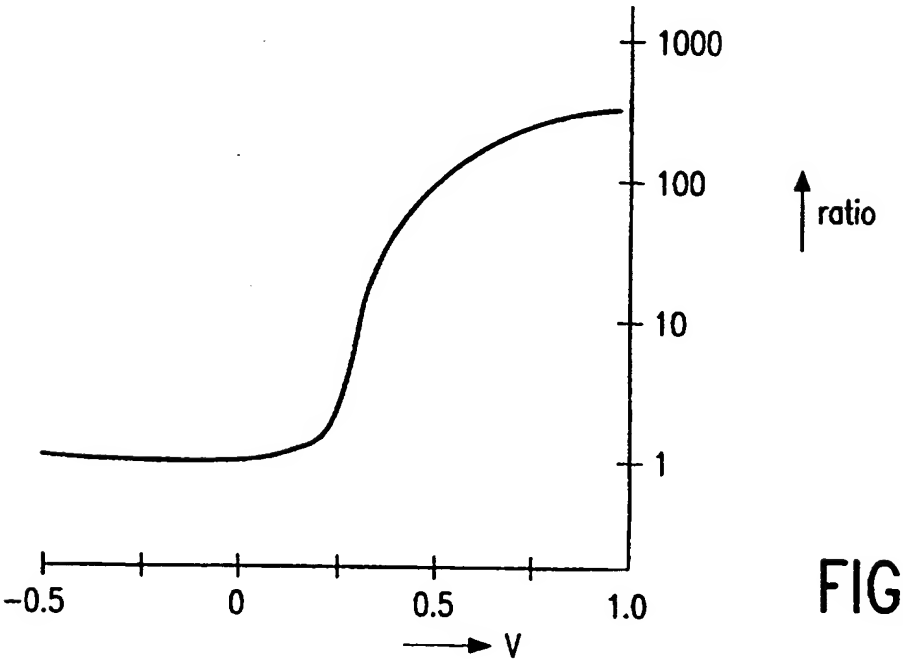

FIG. 5

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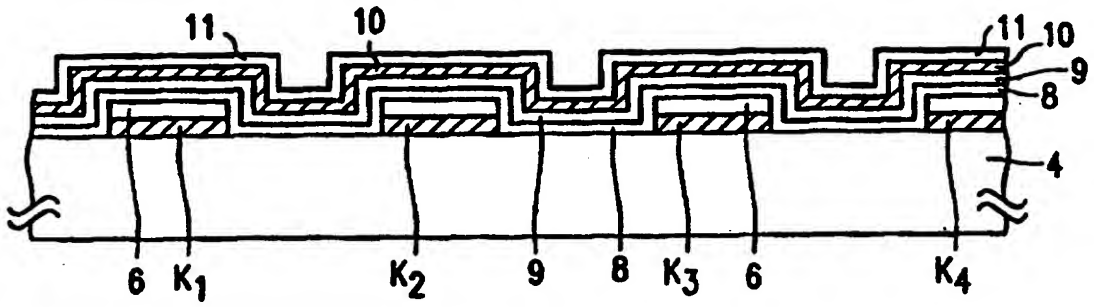

(57) Abstract

The invention relates to an erasable non-volatile memory in which a diode is formed at each point of intersection between the x-selection lines (K_i) and y-selection lines (R_j), of which diode the anode and cathode are conductively connected to the x- and y- selection lines. The diodes are formed in hydrogenated amorphous silicon or silicon compounds such as amorphous $Si_{1-x}Ge_x$. Writing takes place by means of a current pulse through selected diodes. The current in the forward direction becomes much lower, for example a few hundred times lower, than in diodes which are not selected, probably owing to degradation in the semiconductor material. The diodes may be returned to their original state again (i.e. be erased) through heating, for example at a temperature of 200 °C during 100 minutes. Preferably, the diodes are formed by Schottky diodes because the characteristic in the reverse direction does not (substantially) change in this type of diode. The Schottky diodes may be formed in the transitional region between the amorphous intrinsic semiconductor material (6) and the selection lines (K_i).

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CA	Canada	**IT**	Italy	**MX**	Mexico	**UZ**	Uzbekistan
CF	Central African Republic	**JP**	Japan	**NE**	Niger	**VN**	Viet Nam
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CI	Côte d'Ivoire	**KP**	Democratic People's Republic of Korea	**NZ**	New Zealand		
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CU	Cuba	**KZ**	Kazakstan	**RO**	Romania		
CZ	Czech Republic	**LC**	Saint Lucia	**RU**	Russian Federation		
DE	Germany	**LI**	Liechtenstein	**SD**	Sudan		
DK	Denmark	**LK**	Sri Lanka	**SE**	Sweden		
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB 97/00582

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H01L 27/115, G11C 17/14, G11C 11/36 // H01L 21/3065, H01L 21/2247
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H01L, G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

DIALOG: 350, 351

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4599705 A (HOLMBERG ET AL), 8 July 1986 (08.07.86), column 4, line 28 - column 5, line 2; column 7, line 38 - column 8, line 51; column 9, line 1 - column 10, line 17, figures 5,6,10-12, column 11, line 48 - column 13, line 17. Claims 1, 16-18,23-25	1-4,6
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A		9
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Y	US 5404007 A (HOTALING), 4 April 1995 (04.04.95), column 4, line 1 - line 39; column 5, line 29 - line 40, figures 5,6	5,7,8
A		1-5,6,9
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[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 November 1997	28 -11- 1997
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Pär Moritz Telephone No. +46 8 782 25 00

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB 97/00582

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	Patent Abstracts of Japan,, abstract of JP,A, 1-196795 ((SHIH) EPSON CORP), 8 August 1989 (08.08.89) --	1-9
A	US 4396998 A (HUNT ET AL), 2 August 1983 (02.08.83), figures 1-3, claims 1,9,18, abstract --	1-9

INTERNATIONAL SEARCH REPORT

Information on patent family members

01/10/97

International application No.
PCT/IB 97/00582

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